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A PARALLEL ARCHITECTURE DESIGN FOR ULTRA-FAST IMAGE ENCRYPTION WITHIN WMSNS

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This paper aims to enhance performances of an image encryption algorithm by designing its parallel architecture, for the embedded computation in SoC (**S**ystem **o**n **C**hip) designs, using the means provided by CPA (**C**onnex **P**arallel **A**rchitecture). Complying with WMSNs' (**W**ireless **M**ultimedia **S**ensor **N**etworks) typical resources constraints and capabilities, *i.e.*, due to a faster and energy efficient design, algorithm's parallel architecture, as proposed and investigated, is proved to be suitable for usage within WMSNs.

Key words: ConnexArray^{TM}, image encryption, algorithm parallelization.

1. INTRODUCTION

With recent advances in wireless communication and embedded computation, large scales WMSNs are emerging in many applications, as shown in [1 – 5], facing with typical issues (*e.g.*, resources constraints and capabilities, *i.e.*, power consumption, QoS assurance, data storage etc.) and specific ones, more related to multimedia contents' processing techniques (*e.g.*, compression, authentication, encryption [6 – 9], respectively, parallel (or) distributed processing of multimedia contents [9 – 15]); and, with the amount of data stored and processed within, approaching or exceeding petabytes each year [10, 15], the problem of distributed storage and (or) parallel computing is addressed, being challenged both by typical WMSNs' constraints (*e.g.*, few storage and power resources, reduced computation capabilities etc.), *resp.*, parallel processing and storage system architecture design itself [10, 15 – 27, 50, 51].

Problem of parallel processing methods enjoys multiple views, *e.g.*, how to decompose a computationally intensive task into many 'small-sized' tasks which are executed on distributed sensors in parallel [10], in which case many similarities between the problems experienced in distributed WSNs and those of many-core systems are found [16], respectively, designing of new in-network processor architectures, tailored specifically to handling computationally intensive tasks at base station and even at sensor node level [28 – 32].

Current status of parallel computation, *„[...] a bad mixture between parallel structures and parallel algorithms [...]*" [33], *„[...] limited by absence of true parallel architectures [...]*" [33] has motivated the research towards designing of an integral parallel architectures for embedded computation [34, 35], making from resulted ConnexArrayTM SoCs, *i.e.*, CA1024 [36] and BA1024 [35 – 37], targeted competitive solution for multimedia content processing within WMSNs.

Among the recent proposals of in-network processor architectures, *e.g.*, [30 – 32], designed as to handle computationally intensive tasks, *e.g.*, image [32] and other types of multimedia content (pre) processing, the ConnexArray^{TM} (*i.e.*, cellular array which performs the intense part of computation, *e.g.*, CA1024 [36], a SoC design which integrates 1024 EUs, *i.e.*, Execution Units, running at 400MHz and with following measured operating performances: 120 GOPS/watt, respectively, 6.25 GOPS/mm^2 [34]) seemed to be the best current viable solution for designing of multimedia content processing algorithms' parallel architecture, *i.e.*, for high speed, quality processing, with respect to WMSNs typical constraints, such as limited power resources.

Block diagram of ConnexArray^{TM} is presented in Fig. 1. Here a linearly connected array of 1024 EUs receives the same instruction for each EU. The instruction is executed in each EU according to its own state. The reduction networks, designed for the most frequently used reduction functions (add, max etc.), sends back to the controller the requested data. An inner global loop, closed over the array, is used to classify the EUs according to the selected Boolean. The IO system works in parallel with and transparent to the main computation. The SoC CA 1024 contains besides the 1024 EUs (60% of the chip area) audio/video interfaces, a network of 4 MIPS and a time-parallel unit (8 16-bit processors) [34].

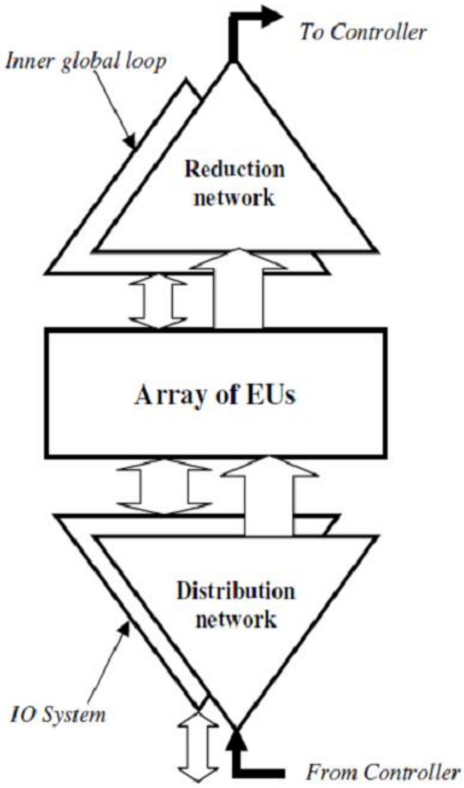


Fig. 1 – The ConnexArrayTM [34].

With the IPA of choice, image encryption algorithm based on Rubik's cube principle [38] was targeted in order to design its parallel architectures for embedded computation, *i.e.*, pursing to demonstrate its suitability for integration within WMSNs (that is, designed and implemented in such manner as to comply WMSNs' typical constraints, *e.g.*, limited power capabilities). Selection of this algorithm is doubly justified:

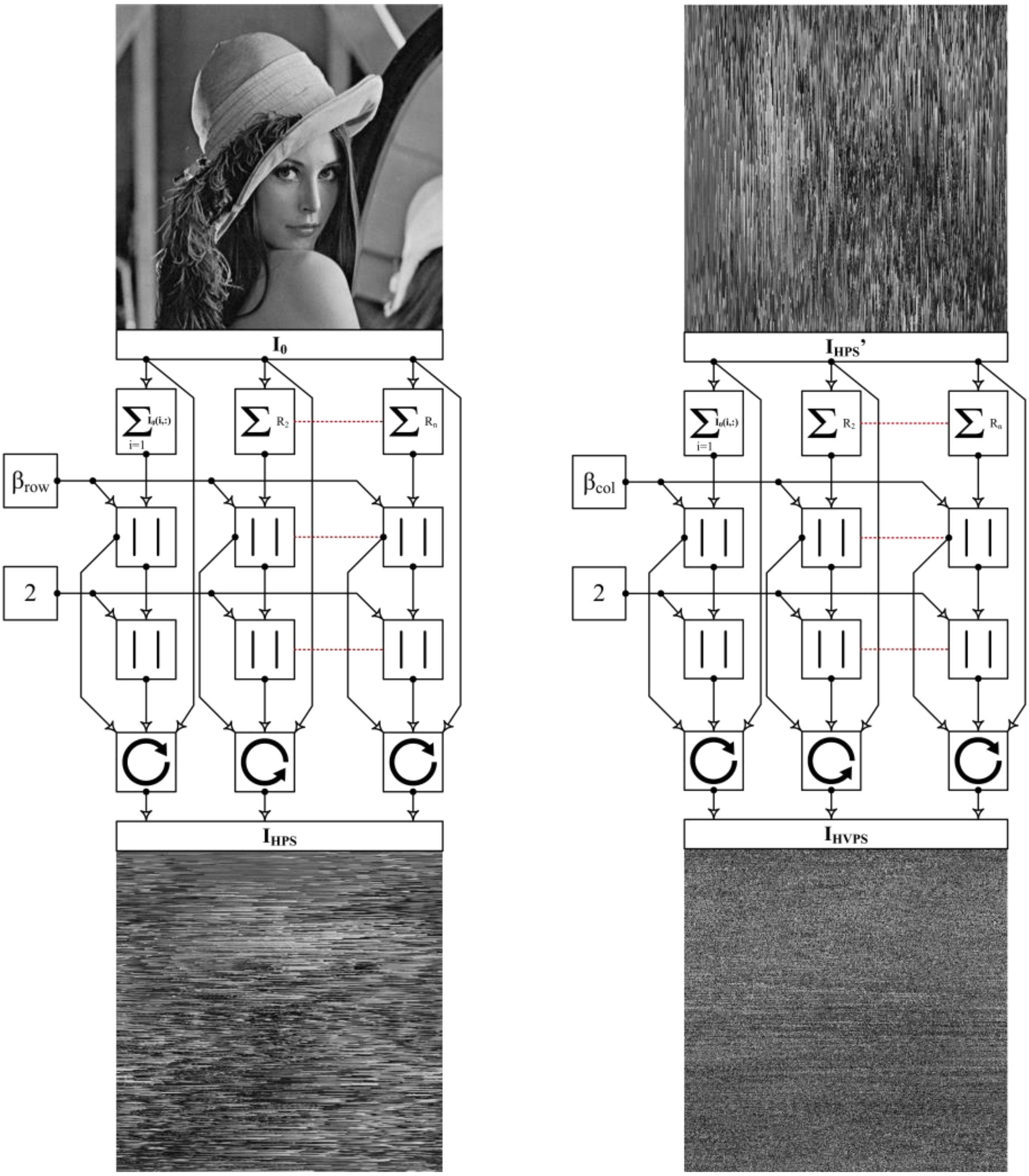
(i) it deals with a priority research interests within WMSNs, *i.e.*, ensuring secure communication mechanisms (since, due to the presence of sensitive multimedia data, *e.g.*, images, audio and (or) video streams containing certain information about individuals, in both an indirect or direct form, as in the case of telemedicine, *e.g.*, [39, 40], they are more vulnerable to security attacks);

(ii)due to its intrinsic design (*i.e.*, mode of operation, as shown in [38]), the selected algorithm is highly parallelizable (*i.e.*, in terms of computational implementation), in contrast with other newly proposed approaches.

Performances of resulted parallel designs were assessed by means of CPA simulator (developed using means offered by DrRacket platform [41]), as to highlight the benefits of using CPA in designing of parallel architecture for newly proposed, computationally intensive, multimedia content processing schemes; targeting the in-network integration, *i.e.*, at sensor node level, within WMSNs.

2. PARALLEL ARCHITECTURE DESIGN OF IMAGE ENCRYPTION ALGORITHM BASED ON RUBIK'S CUBE PRINCIPLE

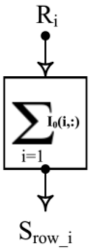
Assuming image's pixels' values pre-loaded in CPA's array, a number of m (where m is equal with image's dimensions, *e.g.*, $m = 512$ in our case) EUs (*i.e.*, Execution Units) are initialized. EUs will execute, simultaneously, a succession of basic operations (*i.e.*, sum of pixels' values, for an entire row R_i; two modulo n operations, where n has the value β_{row} or β_{col}, depending on pixels' shuffling direction, respectively, 2; and one row rotation, either to the left or to the right), in order to complete image's pixels shuffling procedure [38]), as shown in Fig. 2.



a b

Fig. 2 – Parallel architecture of the image encryption algorithm based on Rubik's cube principle – the scrambling procedure: a) first step; b) second step.

Preliminary information about each building block (*i.e.*, the input and output values, the associated CPA functions[1] etc.) are as follows:

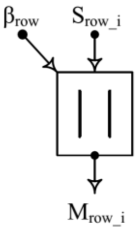


% computes the sum of all elements in row i

Input(s): CPA's array vector i, representing image's row$i$
Output:sum of all elements in row i, *i.e.*, $S_{row\_i} = \sum_{j=1}^{m} I_0(i,j)$; *(review [38])*

Associated CPA function:

(RedAddAll i)**OR**(ResetActive) followed by (RedAdd i).

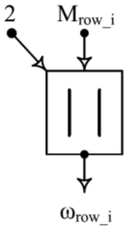


% computes modulo β_{row} of S_{row_i}

Input(s):sum of all elements in row i, *i.e.*, S_{row_i} and β_{row}
Output:modulo β_{row} of S_{row_i}, *i.e.*, $M_{row\_i} = S_{row\_i}(\mathrm{mod}\beta_{row})$; *(review [38])*

Associated CPA function:

(Remainder (RedAddAll i)β_{row}).

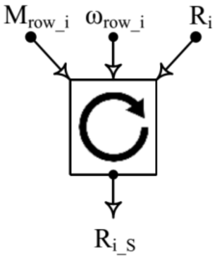


% computes modulo 2 of M_{row_i}

Input(s): modulo β_{row} of S_{row_i}, *i.e.*, M_{row_i} and 2
Output: modulo 2 of M_{row_i}, *i.e.*, $\omega_{row\_i} = M_{row\_i}(\mathrm{mod}\ 2)$; *(review [38])*

Associated CPA function:

(Remainder (Remainder (RedAddAll i) β_{row}) 2).



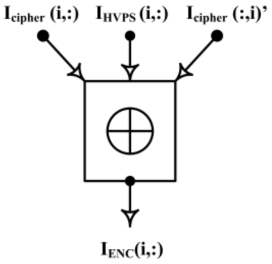
% circular-shift of row i, with M_{row_i}steps, either to the left or to the right, that is, depending on the value of ω_{row_i}; (review [38])

Input(s): ω_{row_i}, M_{row_i} and R_i

Associated CPA function:

```
(if (= (Remainder (Remainder (RedAddAll i) $\beta_{row}$) 2) 0)
    (RotateLeft  (Remainder (RedAddAll i) $\beta_{row}$)  i)
    (RotateRight (Remainder (RedAddAll i) $\beta_{row}$)  i)   ).
```

Fig. no. 3 showcases the parallel architecture of the module which handles the ciphering procedure. In this stage another building block appears (i.e., the bitwise XOR logical operator - based image ciphering block).



% image ciphering; (review [38])

Input(s): $I_{HVPS}(i,:)$, $I_{Cipher}(:,i)'$ and $I_{Cipher}(i,:)$, *i.e.*, rows' pixels from the shuffled image, associated matrix, *resp.*, from the ciphering matrix

Output:
ciphered image, *i.e.*, $I_{ENC}(i,:) = I_{HVPS}(i,:) \oplus I_{Cipher}(i,:) \oplus I_{Cipher}(:,i)'$

Associated CPA function:
(Xor (Xor (Vec i) $\mathrm{I}_{\mathrm{Cipher}}(\mathrm{i},:)$) $\mathrm{I}_{\mathrm{Cipher}}(:,\mathrm{i})'$).

[1] Full length articles and teaching materials about CPA (i.e., including description of the above functions' primitives) can be found at http://arh.pub.ro/gstefan/

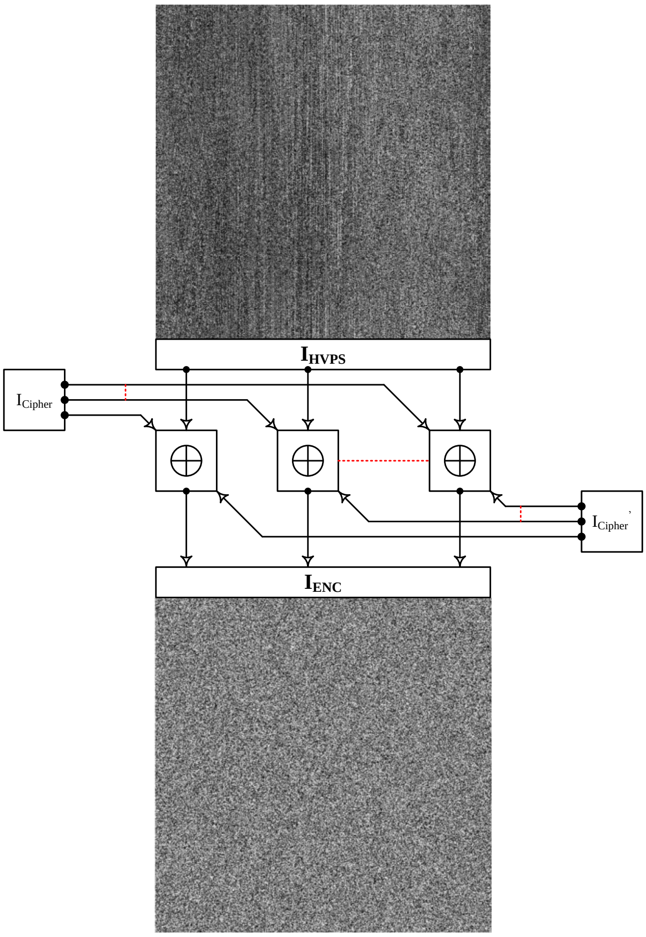


Fig. 3 – Parallel architecture of the image encryption algorithm based on Rubik's cube principle – the ciphering procedure.

3. PERFORMANCES ASSESSMENT

With EU's $Cycles_{Array} = 8$ and $Cycles_{Controler} = 99$ (*i.e.*, spent on the execution of basic operations mentioned above), maximum total number of cycles required to complete image's shuffling procedure can be evaluated using (1). To resulted number of cycles, extra 10% cycles are added (*i.e.*, being attributed to the transparent system's controller operations). Within (1), $Cycles_{Shift}$ is evaluated using (2). Here, l_{gray} represent image's maximum possible gray level's value, *i.e.*, 256, and thus evaluating the worst case scenario, that is, image's rows and columns are shifted with the maximum possible number of steps.

$$Total_{Cycles} = \alpha \cdot 2 \cdot \left(Cycles_{Array} + Cycles_{Controler} + Cycles_{Shift}\right) + 10\% \tag{1}$$

$$Cycles_{Shift} = \max\left(\left(\mathrm{l_{gray}} \cdot \mathrm{m}(\mathrm{mod}\,\beta_{row})\right), \left(\mathrm{l_{gray}} \cdot \mathrm{m}(\mathrm{mod}\,\beta_{col})\right)\right) \tag{2}$$

Knowing $Cycles_{Array} = 4$ (*i.e.*, supplementary number of machine cycles necessary to complete the image's ciphering procedure, that is, second stage of image encryption algorithm), the total number of cycles required to complete the encryption scheme is evaluated at the value of $6230\ cycles/image$.

Previously, it was assumed that image's pixels' values were pre-loaded in CPA's array. But, in order to make a complete and accurate evaluation of the proposed parallel design's performances, I/O bound hypothesis must be checked.

Considering I/O data transfers performed with a rate of 256 *bit/cycle*, *i.e.*, 32 *byte/cycle*, which implies 16 *cycles/vector* (where, vector's dimension is 512 *bytes i.e.*, image's dimension), a number of 8192 *cycles* are required for image's pre-loading stage. One can conclude that proposed parallel architecture is at I/O bound limit and, further, use this value for other performance's numerical evaluation.

In numbers, proposed parallel algorithm's design presents with following performances:

(i) knowing that processes of pre-loading a 512×512 image, respectively, of encrypting it are transparent one to each other (*i.e.*, they could be done in parallel, as also); with an average of 8192 *cycles/image*, by means of CPA, images are processed at a rate of 32 *pixels/cycle*.

(ii) considering use of the CA1024 SoC, with the system clock at 450 MHz (*i.e.*, with an equivalent time of 18.204 μs required to encrypt an image), a rate of 55 *Kframes/s* can be achieved.

Above improvements in the processing time, i.e., resulted encryption system is approximately 2000 times faster, in comparing with the original implementation [38], come with the following explanations:

(i) ConnexArray^{TM}, intrinsically designed to work with buffers (*i.e.*, data load is predictive and transparent) instead of cache memories, excludes, *e.g.*, the 'miss cache' possibility (*i.e.*, time consuming exceptional conditions);

(ii) as seen in Fig. no. 2 and Fig. no 3, algorithms' sequentially is replaced with multiple, parallel, blocks (*i.e.*, processing, at the same time, different image parts) and, by doing this, 'for' - type loops are avoided.

In terms of scalability, *i.e.*, how the input images' size influences the above performances (from throughput's rates point of view), taking into consideration that the actual images' processing speed is bounded by I/O data transfers, with the proposed parallel architecture for image encryption, the following rates can be achieved roughly: 3.46 Gbps (*i.e.*, for square images of the size *m=1024* pixels), 115.34 Gbps (*i.e.*, for square images of the size *m=512* pixels) and 344.45Gbps (*i.e.*, for square images of the size *m=256* pixels and fully pipelined implementation, that is, four images are simultaneously processed). Thus, with much less power consumption (*i.e.*, 160mW, on average), proposed implementation approaches comparable performances with other reported results (that is, of classical or new chaos-based algorithms, designed on different FPGA, multiple CPU or GPU based architectures), *i.e.*, [42-49].

4. CONCLUDING REMARKS

Nowadays designing of integral parallel architectures (targeting embedded computation) is a key research interest, motivated in the field of WMSNs by the amount of data stored and processed within. These IPAs, as all the algorithms implemented within, must be tailored specifically to handle computationally intensive tasks at base station and even at sensor node level, with respect to typical WMSNs' constraints (*i.e.*, power resources, computational capabilities etc.).

Whilst, in previous paper, research work was focused on designing of new multimedia contents' (*i.e.*, still images) processing schemes (*i.e.*, encryption), identifying ConnexArrayTM as an efficient and competitive IPA approach for the embedded computation, present paper has sought to design its parallel architecture. With the IPA of choice (*i.e.*, CA1024), in conjunction of CPA's CAD simulator, the previously proposed image processing algorithms was targeted, in order to design its parallel architecture, *i.e.*, image encryption algorithm based on Rubik's cube principle.

Performances' analysis highlighted that the mix between CPA (*i.e.*, due to its reduced power consumption, in comparison with computing capabilities, that is, 120 GOPS/watt) and proposed image processing schemes (*i.e.*, with highly parallelizable concept), is suitable for integration within WMSNs (due to fast time execution and low power consumption, *i.e.*, the two main operational constraints faced within WMSNs exploitation).

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