THE PUBLISHING HOUSE
OF THE ROMANIAN ACADEMY

PROCEEDINGS OF THE ROMANIAN ACADEMY, Series A,
Volume 12, Number 4/2011, pp. 315–323

TRAPPING ASPECTS IN SILICON-BASED NANOSTRUCTURES

Magdalena Lidia CIUREA

National Institute of Materials Physics, P.O. Box MG-7, 077125 Magurele, Romania
E-mail: ciurea@infim.ro

Trapping aspects in two typical silicon-based nanostructures are investigated. Both 1D nanocrystalline porous silicon structures and 2D (nc-Si/CaF2)50 multilayered structures are considered. The curves of relaxation current versus temperature were obtained using the thermally stimulated currents method without external bias. Two types of maxima (rather broad maxima and spikes) were experimentally evidenced. The spikes are due to the stress-induced traps and their parameters are temperature dependent. To describe the trapping-detrapping-retrapping processes, a general model was proposed. The temperature dependence of stress-induced trap concentrations was described by a power law and the corresponding temperature dependence of cross-sections by a Gaussian law. The model was successfully applied on available experimental data.

Key words: Charge carriers trapping, Multilayers, Traps, Nanocrystalline silicon.

1. INTRODUCTION

The trapping processes play an important role in the electrical transport and phototransport as well as in the light absorption and emission in nanostructured materials and devices. They influence the behavior of the nanostructures and modify the device parameters and consequently the functioning of the devices in an useful or an useless way [1−18].

In the nanostructured materials and particularly, in silicon-based nanostructures, specific aspects of trapping phenomena appear. Thus, the trapping processes are dominated by the traps located at the surface/interface due to the big area/volume ratio, that can reach the value of 10^8 m^{-1} for nanocrystals. These surface/interface traps are formed by the adsorption, the dangling bonds, and the internal stresses induced by lattice misfit [19−26]. In multilayered structures some misfits are produced by the difference between dilatation coefficients and they only act during the cooling or heating the nanostructure. Obviously, the parameters of these traps depend on the cooling/heating regime.

During the past few decades, considerable progress regarding the properties of Si-based nanostructures and devices, influenced by the presence of traps was achieved. The most investigated trap centers are related to Si/SiO_2 interfaces in 2D nanostructures or in devices containing 2D layers. In Ref. [27] the authors use an enhanced spectroscopic charge pumping method to study the Si/SiO_2 interface states in submicron sized MOSFETs (metal-oxide-silicon-field-effect-transistors) with 5.5 nm SiO_2 gate dielectrics. The density of states was electrically measured. They demonstrate that the Si/SiO_2 interface states are mainly of amphoteric P_b center type. The P_b centers, identified by the double peak response signature, are completely different from bulk trap contamination. The Si/SiO_2 interface traps were also investigated in submicron MOSFETs [28] using both charge pumping and random telegraph signal techniques. This study is very important because the presence of traps at the interface between the two gate oxides (a tunnel oxide of 0.8 – 1.2 nm and a deposited high temperature oxide of about 8 nm) produces variations in the drain current. The authors found some hundred fast traps located at this interface and determined their characteristics, i.e. energy position within the silicon bandgap, capture cross section and position within the gate oxide. CMOS (complementary MOS) scaling generates undesirable phenomena, e.g. short channel effect, tunneling leakage and parameter fluctuation [24]. If a charge trap layer is positioned on an arch gate silicon fin in an arch gate structure, the electric field at the tunnel oxide is enhanced and it is reduced at the control oxide, while increasing the effective width of the channel between the source and drain. The study of defects in Si/SiO_2 structures is

made by analyzing of capacitance-voltage ($C - V$) and conductance-voltage ($G - V$) characteristics versus frequency [29]. They are located in ultrathin (~ 10 nm) oxide grown by thermal oxidation at low temperature of hydrogenated Si with orientations (100) and (111), obtained by the hydrogen plasma exposure of Si wafer priorly oxidized. The $C - V$ and $G - V$ characteristics evidence different defects, ones related to interface traps (located in Si gap), the others related to border traps (deeply located in the growing oxide), and the third to bulk Si traps. It was shown that the precursors for trap formation are defects present in less dense Si surface region which is very thin, that contain voids produced during hydrogenation. During oxidation process they are incorporated in the oxide. Conventional silicon MOS ($Al/SiO_2/Si$ MIS) capacitors (interface states) were used, together with proton implanted GaAs Schottky diodes (bulk traps), in order to experimentally test a method, proposed in Ref. [30], which discerns between interface states and bulk traps. The SiO_2 layer was grown by a dry thermal oxidation and has a thickness of 75 nm. The peak related to interface states, in two deep-level transient spectroscopy (DLTS) spectra measured at fixed pulse voltage, is recognized by its shift towards higher temperatures with the increase of the reverse voltage modulus, whereas the one related to bulk traps remains the same or it moves towards lower temperature.

In order to have a better performance of scaled MOSFET devices, one can use oxidized strained Si layers on Si_xGe_{1-x} virtual substrates as an alternative to the standard Si/SiO_2 interface [25]. These layers have a lower density of both interface traps and near interface traps than Si/SiO_2 interface. Ioannou-Sougleridis *et al.* [25] studied the electrical properties of strained-Si/relaxed Si_xGe_{1-x} heterostructure, consisting of p++ boron doped Si wafer, epitaxial p-type silicon layer, graded Si_xGe_{1-x}, $Si_{0.78}Ge_{0.22}$ layer, and strained 13 nm thick Si layer. $C - V$ characteristics were measured at different frequencies, as well as conductance characteristics vs. frequency for different gate voltages and at different temperatures. The authors of Ref. [25] evidenced the presence of interfacial traps with large density. Their density is dependent on the oxidation process, increasing with the increase of the oxidation time. On the other hand, when the strained Si layer is exhausted by the oxidation process, the density reduces. This proves that the strained silicon/$Si_{0.78}Ge_{0.22}$ interface is a main source of these defects.

Trapping of carriers in nanocrystalline silicon (nc-Si) is intensively studied in the literature [16, 31] due to its possible applications as memory devices (nanocrystals charge trap memory application) [2, 3]. Carriers are trapped on the quantum confinement levels of a nanodot [32]. Charge DLTS (Q-DLTS) technique was used in order to study the charging of nc-Si embedded in a SiO_2 matrix [32]. Two deep traps were detected, these levels being associated with the nanocrystals due to carrier trapping on the quantum confinement levels of a nanodot. Lin *et al.* [16] also studied the memory properties and charge effect in isolated nc-Si, obtained by a dewetting process of a thin Si layer deposited on a tunneling (5 nm thick) SiO_2 layer. They used the conductive tip of a scanning capacitance microscop to apply DC bias and thus to individually inject charges (electrons or holes) into Si nanocrystals, which were then recorded by the scanning capacitance spectroscopy images. The trapping of these charges will produce a capacitance modification which can be easily detected at the nanometer scale with these techniques.

Charge trapping properties are also interesting in Ge quantum dots. Buljan *et* al. [33] studied trapping properties in two bilayer ($Ge+SiO_2$)/SiO_2 films consisting of Ge quantum dots embedded in a SiO_2 matrix separated by a SiO_2 layer with 5 nm thickness. These films were deposited by magnetron sputtering on a rippled substrate and annealed either in vacuum or forming gas. Thus, self-ordered Ge quantum dots were obtained. $C - V$ characteristics taken at high-frequency and DLTS spectra were recorded in order to describe the charge trapping. The authors of Ref. [33] showed that in films annealed in forming gas the charge trapping in quantum dots is dominant, while in those annealed in vacuum, $Si-SiO_2$ interface trapping occurs.

In this paper we present and discuss the trapping phenomena in two Si-based nanostructures, one being a 1D nanocrystalline porous silicon (nc-PS) structure and the other one a 2D $(nc-Si/CaF_2)_{50}$ multilayered structure. The experimental curves of the relaxation current versus temperature were obtained by thermally stimulated currents method without external bias. A model to describe the relaxation currents was proposed and experimental results were discussed in the framework of this model.

2. EXPERIMENTAL RESULTS

Nanocrystalline porous silicon films were prepared by the classical method of electrochemical etching, followed by photochemical processing, from (100) p-type silicon (Si) wafer [34−36]. This preparation

procedure assures forming of 1D nanostructures in which nc-Si wires have diameters between 1 and 3 nm and lengths of micrometer order of magnitude. 2D multilayered structures of $(\text{nc-Si}/CaF_2)_{50}$ were prepared by molecular beam epitaxy and they are formed by 50 pairs of nc-Si and CaF_2 layers, each layer with thickness g = 1.6 nm [22, 37−39]. All the investigated structures have sandwich geometry of electrodes with semitransparent top electrode, so that all the non-homogeneities parallel to the top electrode are averaged over the top electrode area A. Consequently, the horizontal trap distribution (parallel to the top electrode) can be considered as homogeneous [22].

As investigation method for trapping processes we choose the method of thermally stimulated currents without external bias (also called optical charging spectroscopy) [40]. This zero-bias method allows the generating of an internal electrical field by illuminating the samples at low temperatures, with a light wavelength λ, chosen in the absorption band. Thus, the photogenerated carriers diffuse in the structure with different velocities ($v_n \neq v_p$) during their lifetime and they are trapped generating a frozen-in electric field. In the Si-based nanostructures investigated in this work, both the absorption length and bipolar diffusion length are greater than the thickness of the film d, and the illumination time is sufficiently long so that the uniform filling (charging) of the traps is achieved. If the absorption length and bipolar diffusion length are smaller than the structure thickness or if the illumination time is not long enough, one obtains a gradient of trap charging. The heating made at a constant rate under no external bias will produce a trap discharge, so that the detrapped carriers move under the internal electric field produced by still trapped carriers. A relaxation current, dependent on the frozen-in electric field, is measured. The movement of the discharge carriers under the electric field produced by still trapped carriers makes this method more sensitive in comparison to classical thermally stimulated current one where during the heating, discharge carriers move under external bias. The experimental current-temperature curves present positive and/or negative maxima and/or shoulders where from, the depth of the trapping levels (activation energies) and trap concentrations are determined.

A typical experimental curve of the relaxation current versus temperature obtained on nc-PS nanostructure is presented in Fig. 1 [41][1]. In order to obtain accurate activation energies, the fractional heating

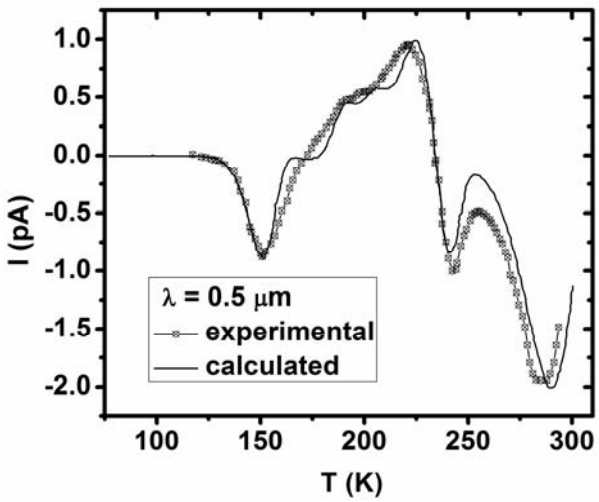

Fig. 1 – Relaxation current versus temperature in nc-PS, for charging wavelength λ = 0.5 μm [41].

procedure was performed. Starting from the lowest measurement temperature T_0, the sample is heated up to the first maximum located at the lowest temperature and kept there until the current almost vanishes, i.e. the trapping level is completely discharged. Then, the sample is cooled down to T_0 and again the sample is heated up to the second maximum and/or shoulder and so on. The retrapping process will produce the appearance of the current maximum after the trapping level corresponding to it is discharged. Using fractional heating procedure, the activation energies obtained from the increasing part of the discharge

[1] Reprinted from Journal of Applied Physics **94** (1), V. Iancu, M.L. Ciurea, M. Draghici, "Modeling of optical charging spectroscopy investigation of trapping phenomena in nanocrystalline porous silicon", 216-223, Copyright (2003), with permission from American Institute of Physics.

currents are $E_{t1}^{\exp} = 0.29\,\text{eV}$, $E_{t3}^{\exp} = 0.47\,\text{eV}$, $E_{t4}^{\exp} = 0.61\,\text{eV}$ and a broad maximum whose activation energy is $E_{t2}^{\exp} = 0.37 \div 0.41\,\text{eV}$. The broad maximum number 2 corresponds to the superposition of two very close trapping levels that can not be experimentally separated.

In 2D $(\text{nc-Si/CaF}_2)_{50}$ structures two types of trapping aspects are evidenced. If the sample is cooled down in quasistatic regime the relaxation current presents maxima typical for normal trapping levels. If the cooling is relatively fast, in the temperature dependence of the relaxation current, several spikes (very sharp ones) are evidenced. These spikes also appear in the curves of relaxation currents although the sample was not illuminated at low temperature (zero curve). This behavior suggests that spikes are due to the misfit produced by the difference between the dilatation coefficients of adjacent layers of nc-Si and CaF_2.

A typical temperature dependence of the relaxation current when the structure was cooled down under a quasistatic regime, measured on 2D $(\text{nc-Si/CaF}_2)_{50}$ structures is presented in Fig. 2 [22][2]. The experimental activation energies obtained from the fractional heating procedure are $E_{t1}^{\exp} = 0.30\,\text{eV}$, $E_{t2}^{\exp} = 0.42\,\text{eV}$, $E_{t3}^{\exp} = 0.44\,\text{eV}$ and $E_{t4}^{\exp} = 0.75\,\text{eV}$. A similar curve when the structure is cooled down relatively fast is illustrated in Fig. 3 [42]. As one can see, the curves contain very sharp spikes in comparison with those due to the "normal" traps that are rather broad, as in Fig. 2. Also, these curves are very noisy so that a procedure of optimal linear smoothing was required to be used [26].

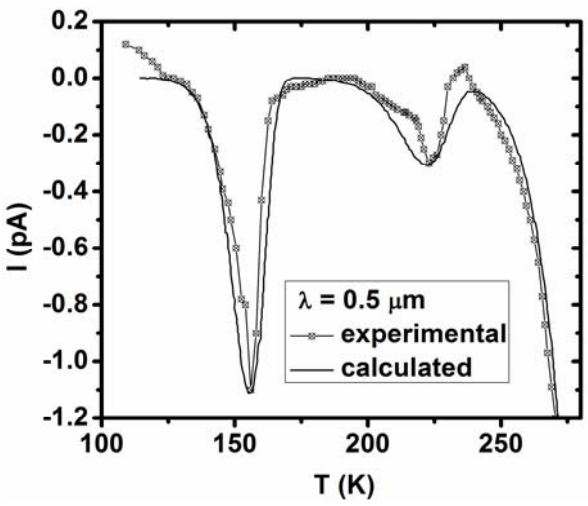

Fig. 2 – Relaxation current versus temperature in $(\text{nc-Si/CaF}_2)_{50}$, for charging wavelength λ = 0.5 μm [22].

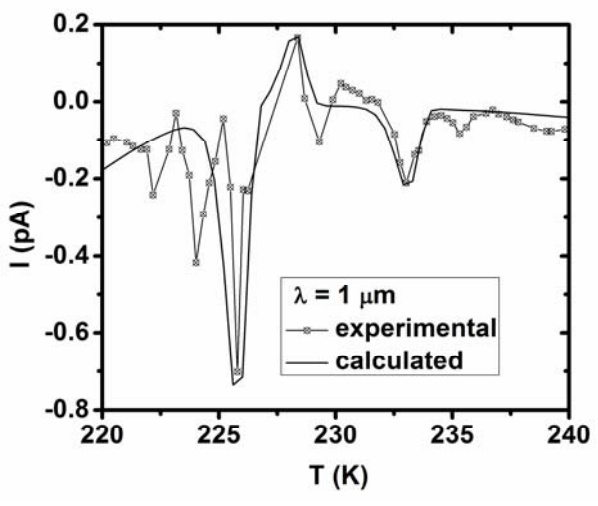

Fig. 3 – Relaxation current versus temperature in $(\text{nc-Si/CaF}_2)_{50}$, for charging wavelength λ = 1 μm [42].

3. THEORETICAL MODELING

In order to describe the relaxation currents obtained without external bias presented in the previous section we proposed a general model discussed in detail in the Refs. 22 and 26.

The hypotheses of the model are the following: (1) the structure thickness *d* (thickness of nc-PS film and $(\text{nc-Si/CaF}_2)_{50}$, respectively) is much smaller than both the absorption length and the bipolar diffusion one, so that the traps are fully filled; (2) the trapping levels have zero width; (3) the cooling is quasistatic in order to evidence "normal" traps or relatively fast to evidence spikes; (4) the heating is quasistatic using a small heating rate β.

Under these assumptions, the trapping, detrapping and retrapping processes are described by the following equations [22, 26]:

[2] Reprinted from Solid-State Electronics **51** (10), M. L. Ciurea, V. Iancu, M. R. Mitroi, "Trapping phenomena in silicon-based nanocrystalline semiconductors", 1328-1337, Copyright (2007), with permission from Elsevier.

$$\left\{1+\sum_{i'}\tau_{ni'}c_{ni'}\left(T\right)\left[N_{ti'}\left(T\right)-n_{ti'}\left(T\right)\right]\right\}\times\frac{\partial}{\partial T}n_{ti}\left(T\right)=-\frac{1}{\beta}c_{ni}\left(T\right)N_{cti}\left(T\right)n_{ti}\left(T\right) \tag{1}$$

for electrons, and analogue for holes:

$$\left\{1+\sum_{j'}\tau_{pj'}c_{pj'}\left(T\right)\left[P_{tj'}\left(T\right)-p_{tj'}\left(T\right)\right]\right\}\times\frac{\partial}{\partial T}p_{tj}\left(T\right)=-\frac{1}{\beta}c_{pj}\left(T\right)P_{vtj}\left(T\right)p_{tj}\left(T\right), \tag{2}$$

where $\tau_n=1/c_nN_t$ and $\tau_p=1/c_pP_t$ are the non-equilibrium carrier lifetime for electrons and holes, respectively, $c_n\left(T\right)=s_n\left(T\right)\tilde{v}_e\left(T\right)$ and $c_p\left(T\right)=s_p\left(T\right)\tilde{v}_h\left(T\right)$ are the capture coefficients with s_n and s_p capture cross-sections, and $\tilde{v}_e\left(T\right)=\sqrt{3kT/m_e^*}$, $\tilde{v}_h\left(T\right)=\sqrt{3kT/m_h^*}$. For normal traps, capture coefficients are given by the thermal velocities, only, and for stress induced traps, the capture cross-sections also depend on the temperature.

$$\Delta n\left(T\right)\equiv n\left(T\right)-n_0\left(T\right)=\sum_i\tau_{ni}c_{ni}\left(T\right)N_{cti}\left(T\right)n_{ti}\left(T\right), \tag{3}$$

$$\Delta p\left(T\right)\equiv p\left(T\right)-p_0\left(T\right)=\sum_j\tau_{pj}c_{pj}\left(T\right)P_{vtj}\left(T\right)p_{tj}\left(T\right). \tag{4}$$

$n_0(T)$ and $p_0(T)$ represent the equilibrium electron and hole concentrations, respectively, and $n_{ti}\left(T\right)$, $p_{tj}\left(T\right)$ represent the concentrations of carriers trapped on the levels i, j.

Here $N_{cti}(T)$ and $P_{vtj}(T)$ are given by the following expressions

$$N_{cti}\left(T\right)=2\left(\frac{m_e^*kT}{2\pi\hbar^2}\right)\exp\left(-\frac{E_c-E_{ti}}{kT}\right),\quad P_{vtj}\left(T\right)=2\left(\frac{m_h^*kT}{2\pi\hbar^2}\right)\exp\left(\frac{E_v-E_{tj}}{kT}\right) \tag{5}$$

for normal traps, and for stress-induced trap concentrations we proposed a temperature dependence according to a power law, as follows

$$N_t\left(T\right)=N_t^{(0)}\left(1-\frac{T}{T_s}\right)^{\gamma_n},\quad P_t\left(T\right)=P_t^{(0)}\left(1-\frac{T}{T_s}\right)^{\gamma_p}, \tag{6}$$

where T_S is the storage temperature, $\gamma_n\geq 1$ and $\gamma_p\leq 4$ are integer exponents.

The frozen-in electric field, under the model hypotheses, and considering that all the traps are located at the interfaces between layers in the case of 2D Si-based nanostructures, is

$$\tilde{E}(T)=\frac{2q+1}{4}\frac{eg}{\varepsilon_0\varepsilon_r}\left[\sum_j p_{tj}(T)-\sum_i n_{ti}(T)\right], \tag{7}$$

with ε_r being the Si and CaF_2 permittivity, for nc-PS and $(\text{nc-Si/CaF}_2)_{50}$ structures, respectively.

The total discharge current is

$$I\left(T\right)=\frac{A}{d}\int_0^d j\left(z,T\right)\mathrm{d}z\equiv A\tilde{j}\left(T\right), \tag{8}$$

where $j(z,T)$ is the current density, and $\tilde{j}\left(T\right)$ is its mean value. The current density $j(z,T)$, as well as the total discharge current, have five terms corresponding to five possible contributions: the Ohmic conduction current density produced by equilibrium carriers ($j_e=\sigma_0\left(T\right)E_z\left(z,T\right)$), the non-equilibrium carrier conduction current density ($j_{ne}=\Delta\sigma\left(z,T\right)E_z\left(z,T\right)$ being the most important term to the discharge current, for Ohmic conduction), the diffusion current density, negligible in the model hypotheses, the displacement

current density and the tunneling current density, both negligible for nc-PS structures, but important for 2D $(nc\text{-}Si/CaF_2)_{50}$ structures (see details in Ref. 22).

In nc-PS structures, the total current is given by the formula

$$I(T)=\frac{A}{d}\int_0^d\left(j_e(z,T)+j_{ne}(z,T)\right)\mathrm{d}z\,, \tag{9}$$

with $\sigma_0(T)=e\left[\mu_n(T)n_0(T)+\mu_p(T)p_0(T)\right]$ and $\Delta\sigma(z,T)=e\left[\mu_n(T)\Delta n(z,T)+\mu_p(T)\Delta p(z,T)\right]$.

In $(nc\text{-}Si/CaF_2)_{50}$ nanostructures, the total current is the sum of displacement and tunneling currents

$$I(T)=I_d(T)+I_t(T)\,, \tag{10}$$

where the displacement current is

$$I_d(T)=\varepsilon_0\varepsilon_r A\beta\frac{\mathrm{d}\tilde{E}}{\mathrm{d}T} \tag{11}$$

and the tunneling current is

$$\begin{aligned}I_t(T)=\mathrm{sign}\left(\tilde{U}\right)\Bigg\{&I_n\left[\left(1-\frac{|\tilde{U}|}{U_n}\right)\times\exp\left(-\alpha_n\sqrt{1-\frac{|\tilde{U}|}{U_n}}\right)-\exp\left(-\alpha_n\right)\right]-\\&-I_p\left[\left(1+\frac{|\tilde{U}|}{U_p}\right)\times\exp\left(-\alpha_p\sqrt{1+\frac{|\tilde{U}|}{U_p}}\right)-\exp\left(-\alpha_p\right)\right]\Bigg\},\end{aligned} \tag{12}$$

with

$$\begin{aligned}&I_n=\frac{enA\tilde{v}_e}{\sqrt{3}}\ \text{ and }\ I_p=\frac{epA\tilde{v}_h}{\sqrt{3}},\\&\alpha_n=\sqrt{\frac{8em_e^*U_n g^2}{\hbar^2}}\,,\quad \alpha_p=\sqrt{\frac{8em_h^*U_p g^2}{\hbar^2}}\,.\end{aligned} \tag{13}$$

In the case of $(nc\text{-}Si/CaF_2)_{50}$ nanostructures, the experimental sharp spikes due to the stress-induced traps are well fitted if a temperature dependence of the capture cross-sections is introduced. For this, we consider that the capture cross-section is proportional to probability distributions, centered on the spike temperature position with a Gaussian form, suggested by the thermodynamical fluctuation theory

$$s_{ni}=s_{ni}^{(0)}\exp\left(-\frac{\left(T-T_{ni}\right)^2}{2W_{ni}^2}\right),\quad s_{pj}=s_{pj}^{(0)}\exp\left(-\frac{\left(T-T_{pj}\right)^2}{2W_{pj}^2}\right). \tag{14}$$

4. DISCUSSION OF RESULTS

The application of our model to the experimental results requires using the activation energies obtained from fractional heating measurements, as start values. For other necessary start parameters such as capture cross-sections and lifetimes we used data from literature. The system of equations (1–2) was solved using Rkadapt solver in a dedicated Mathcad 14.0 program.

The fit of the relaxation current curves obtained for nc-PS structures is presented in Fig. 1. In these structures the retrapping process is weak, so that a simplified model can be used as a result of decoupling of equations (1)-(2). The data obtained from fitting are presented in Table 1 [40, 41].

Table 1

Parameters of trapping levels obtained in nc-PS structures

$E_{ti}^{\exp}$ (eV)	$N_t\ (P_t)$ (10^{11} cm^{-3})	s (10^{-18} cm^2)	τ (ns)	E_{ti}^{m} (eV)
0.29	18.0	3.0	50	0.30
0.37 – 0.41	15.0	3.0	50	0.37
	2.5	1.5	50	0.41
0.47	14.0	0.9	50	0.47
0.61	0.85	3.0	150	0.61

One can see from Table 1 that the broad maximum ($E_{t2}^{\exp} = 0.37 \div 0.41\,\text{eV}$) was split in two trapping levels with the activation energies $E_{t2'}^{m} = 0.37$ eV and $E_{t2''}^{m} = 0.41$ eV. The identification of trapping type levels (traps for electrons or holes) can be determined taking into account the differences between the mobilities and effective masses between electrons and holes. Thus, the traps corresponding to E_{t1}^{m}, $E_{t2'}^{m}$ and E_{t4}^{m} are traps for holes, while the others are traps for electrons. All the traps, but E_{t4}^{m}, are located on the surface of the nanowires, E_{t4}^{m} being located in their volume.

In Table 2 are presented the parameters of "normal" traps as they result from curves illustrated in Fig. 2 for $(\text{nc-Si/CaF}_2)_{50}$ structures [22]. Looking at parameter values from both Tables 1 and 2, one can observe that they are very close to each other, therefore we can conclude that they are specific to nc-Si-based structures (trap concentrations are dependent on the structure).

Table 2

Parameters of "normal" trapping levels obtained in $(\text{nc-Si/CaF}_2)_{50}$ structures (curve from Fig. 2)

$E_{ti}^{\exp}$ (eV)	$N_t\ (P_t)$ (10^{14} cm^{-3})	s (10^{-18} cm^2)	τ (ns)	γ	E_{ti}^{m} (eV)
0.30	66.00	1.70	400	4	0.30
0.42	26.00	0.41	400	4	0.42
0.44	0.29	1.00	180	0	0.44
0.75	55.00	1.50	400	0	0.72

As it was already mentioned in the preceding section on theoretical modeling, in order to fit the experimental sharp spikes, we introduced a temperature dependence of the capture cross-sections. Thus, by introducing formula (14) in the system of equations (1–2), the sharp spikes are well fitted (with Gaussian width of 2 K) as one can see in Fig. 3. The results are presented in Table 3. We also notice that only three maxima and minima were fitted, the others being too close, therefore they are insignificant.

Table 3

Parameters of the stress-induced traps obtained in $(\text{nc-Si/CaF}_2)_{50}$ structures (curve from Fig. 3)

T_n, T_p (K)	$N_t^{(0)}, P_t^{(0)}$ (10^{15} cm^{-3})	$s^{(0)}$ (10^{-18} cm^2)	E_{ti}^{m} (eV)
229	6.8	50	0.42
232	0.9	50	0.44
236	3.14	50	0.45

5. CONCLUSIONS

In this paper we have investigated trapping processes in both 1D nc-PS structures and 2D (nc-$Si/CaF_2)_{50}$ multilayered structures. We used the method of thermally stimulated current without external bias, recording the temperature dependence of relaxation currents. Two different shapes of maxima were experimentally evidenced in the curves of relaxation current versus temperature. Some of them are rather broad (already a well known result), and they are evidenced in both structures, whereas the other maxima are sharp spikes that appear in 2D (nc-$Si/CaF_2)_{50}$ multilayered structures, only. We demonstrated that spikes are given either by discharging of stress-induced traps produced by the lattice misfit or by the difference between dilatation coefficients.

A general model for trapping-detrapping-retrapping processes was proposed in order to describe both types of maxima in the investigated structures. A system of non-linear coupled differential equations describes these processes. It was experimentally proved that the parameters of spikes are dependent on cooling rate. Thus, we proposed a power law for the temperature dependence of the stress-induced traps concentration, and a Gaussian law for the temperature dependence of their capture cross-section.

We applied the model to experimental results and a good fit was obtained. From this model, the parameters of traps which are present in the two investigated Si-based nanostructures were determined. Finally one notices that some of the traps investigated in this work are in fact typical for Si-based nanostructures.

ACKNOWLEDGEMENTS

The contribution to this work was supported by the Romanian National Authority for Scientific Research through the CNCSIS –UEFISCDI, Contract PCCE-ID-76.

REFERENCES

1. I.V. ANTONOVA, V.P. POPOV, V.I. POLYAKOV, A.I. RUKOVISHNIKOV, *Traps with Near-Midgap Energies at the Bonded Si/SiO_2 Interface in Silicon-on-Insulator Structures*, Semiconductors, **38**, pp. 1394–1399, 2004.
2. R.J. WALTERS, G.I. BOURIANOFF, H. A. ATWATER, *Field-effect electroluminescence in silicon nanocrystals*, Nat. Mater., **4**, pp. 143–146, 2005.
3. S. HUANG, S. ODA, *Charge storage in nitrided nanocrystalline silicon dots*, Appl. Phys. Lett., **87**, *1–3*, pp. 173107, 2005.
4. M. HOFHEINZ, X. JEHL, M. SANQUER, G. MOLAS, M. VINET, S. DELEONIBUS, *Individual charge traps in silicon nanowires - Measurements of location, spin and occupation number by Coulomb blockade spectroscopy*, Europ. Phys. J. B, **54**, pp. 299–307, 2006.
5. A. KHAN, A. FREUNDLICH, *Carrier loss channels for non-collected carrier in $InAs_xP_{1-x}$ /InP multiquantum well solar cells*, Appl. Phys. Lett., **88**, *1–3*, pp. 103504, 2006.
6. J.W. KIM, G.H. SONG, J.W. LEE, *Observation of minority-carrier traps in InGaN/GaN multiple-quantum-well light-emitting diodes during deep-level transient spectroscopy measurements*, Appl. Phys. Lett., **88**, *1–3*, pp. 182103, 2006.
7. I.J. CHEN, T.T. CHEN, Y.F. CHEN, T.Y. LIN, *Nonradiative traps in InGaN/GaN multiple quantum wells revealed by two wavelength excitation*, Appl. Phys. Lett., **89**, *1–3*, pp. 142113, 2006.
8. J.-S. LEE, J.H. CHO, C.Y. LEE, I.P. KIM, J.J. PARK, Y.-M. KIM, H.J. SHIN, J.G. LEE, F. CARUSSO, *Layer-by-layer assembled charge-trap memory devices with adjustable electronic properties*, Nat. Nanotechnol., **2**, pp. 790–795, 2007.
9. K.P. MCKENNA, A.L. SHLUGER, *Electron-trapping polycrystalline materials with negative electron affinity*, Nature Mater., **7**, pp. 859–862, 2008.
10. S. PREZIOSO, A. ANOPCHENKO, Z. GABURRO, L. PAVESI, G. PUCKER, L. VANZETTI, P. BELLUTTI, *Electrical conduction and electroluminescence in nanocrystalline silicon-based light emitting devices*, J. Appl. Phys., **104**, *1–8*, pp. 063103, 2008.
11. D.U. LEE, T.H. LEE, E.K. KIM, J.-W. SHIN, W.-J. CHO, *Analysis of charge loss in nonvolatile memory with multi-layered SiC nanocrystals*, Appl. Phys. Lett., **95**, *1–3*, pp. 063501, 2009.
12. S. KUGE, H. YOSHIDA, *Local mapping of interface traps in HfSiO/Si structure by scanning capacitance microscopy using dV/dC signal*, J. Appl. Phys., **105**, *1–4*, pp. 093708, 2009.
13. D. MENICHELLI, R. MORI, M. SCARINGELLA, M. BRUZZI, *Zero-bias thermally stimulated currents (ZB-TSC) spectroscopy of deep traps in irradiated silicon particle detectors*, Nucl. Instrum. Meth. A, **612**, pp. 530–533, 2010.
14. R. DARWICH, P. ROCA I CABARROCAS, *Characterization of defects in hydrogenated amorphous silicon deposited on different substrates by capacitance techniques*, Thin Solid Films, **519**, pp. 5473–5480, 2011.
15. S.K. ESTREICHER, D. BACKLUND, T.M. GIBBONS, *Theory of defects in Si and Ge: Past, present and recent developments*, Thin Solid Films, **518**, pp. 2413–2417, 2010.
16. Z. LIN, G. BREMOND, F. BASSANI, *Memory properties and charge effect study in Si nanocrystals by scanning capacitance microscopy and spectroscopy*, Nanoscale Res. Lett, **6**, *1–5*, pp. 163, 2011.

17. Y. YONAMOTO, Y. INABA, N. AKAMATSU, *Detection of nitrogen related traps in nitrided/reoxidized silicon dioxide films with thermally stimulated current and maximum entropy method*, Appl. Phys. Lett., **98**, *1–3*, pp. 232906, 2011.
18. N. HAMDAOUI, R. AJJEL, B. SALEM, M. GENDRY, H. MAAREF, *Coulomb charging effect of electrons in InAs/InAlAs quantum dots studied by capacitance techniques*, Physica B, **406**, pp. 3531–3533, 2011.
19. D. A. FAUX, J. R. DOWNES, AND E. P. O'REILLY, *Analytic solutions for strain distributions in quantum-wire structures*, J. Appl. Phys., **82**, pp. 3754–3762, 1997.
20. A. BENFDILA, Proceedings of the 1st International Workshop on Semiconductor and Nanocrystals, SEMINANO 2005, Budapest, 10–12 September 2005, edited by B. Pödör, Zs. Horvath, and P. Basa, published by MTA MFA (Research Institute for Technical Physics and Materials Science of the Hungarian Academy of Sciences), Budapest, **1**, pp. 123–126, 2005.
21. J. F. CHEN, C. H. CHIANG, P. C. HSIEH, J. S. WANG, *Analysis of strain relaxation in GaAs/InGaAs/GaAs structures by spectroscopy of relaxation-induced states*, J. Appl. Phys., **101**, *1–4*, pp. 033702, 2007.
22. M.L. CIUREA, V. IANCU, M.R. MITROI, *Trapping phenomena in silicon-based nanocrystalline semiconductors*, Solid-State Electron., **51**, pp. 1328–1337, 2007.
23. S. DHAMODARAN, A. P. PATHAK, A. TUROS, R. KESAVAMOORTHY, B. SUNDARAVEL, *Structural and compositional analysis of strain relaxed InGaAs/InP multi quantum wells*, Nucl. Instrum. Methods Phys. Res. B, **266**, pp. 1908–1911, 2008.
24. B.-G. PARK, J.Y. SONG, J.P. KIM, H. JEONG, J.H. LEE, S. CHO, *Nanosculpture: Three-dimensional CMOS device structures for the ULSI era*, Microelectron. J., **40**, pp. 769–772, 2009.
25. V. IOANNOU-SOUGLERIDIS, N. KELAIDIS, D. SKARLATOS, C. TSAMIS, S.N. GEORGA, C.A. KRONTIRAS, PH. KOMNINOU, TH. SPELIOTIS, P. DIMITRAKIS, B. KELLERMAN, M. SEACRIST, *Influence of thermal oxidation on the interfacial properties of ultrathin strained silicon layers*, Thin Solid Films, **519**, pp. 5456–5463, 2011.
26. M.L. CIUREA, S. LAZANU, I. STAVARACHE, A.-M. LEPADATU, V. IANCU, M.R. MITROI, R.R. NIGMATULLIN, C.M. BALEANU, *Stress-induced traps in multilayered structures*, J. Appl. Phys., **109**, pp. 013717, 2011.
27. J.T. RYAN, L.C. YU, J.H. HAN, J.J. KOPANSKI, K.P. CHEUNG, F. ZHANG, C. WANG, J.P. CAMPBELL, J.S. SUEHLE, *Spectroscopic charge pumping investigation of the amphoteric nature of Si/SiO_2 interface states*, Appl. Phys. Lett., **98**, *1–3*, pp. 233502, 2011.
28. N. SGHAIER, L. MILITARU, M. TRABELSI, N. YACOUBI, A. SOUIFI, *Analysis of slow traps centres in submicron MOSFETs by random telegraph signal technique*, Microelectron. J., **38**, pp. 610–614, 2007.
29. S. ALEXANDROVA, A. SZEKERES, E. HALOVA, *Defects in SiO_2/Si Structures Formed by Dry Thermal Oxidation of RF Hydrogen Plasma Cleaned Si*, IOP Conf. Ser. Mater. Sci. Eng., **15**, *1–4*, pp. 012037, 2010.
30. A.V.P. COELHO, M.C. ADAM, H. BOUDINOV, *Distinguishing bulk traps and interface states in deep-level transient spectroscopy*, J. Phys. D: Appl. Phys., **44**, *1–7*, pp. 305303, 2011.
31. A. FISSEL, A. LAHA, E. BUGIEL, D. KÜHNE, M. CZERNOHORSKY, R. DARGIS, H.J. OSTEN, *Silicon in functional epitaxial oxides: A new group of nanostructures*, Microelectron. J., **39**, pp. 512–517, 2008.
32. I.V. ANTONOVA, V.A. VOLODIN, E.P. NEUSTROEV, S.A. SMAGULOVA, J. JEDRZEJEWSI, I. BALBERG, *Charge spectroscopy of Si nanocrystallites embedded in a SiO_2 matrix*, J. Appl. Phys., **106**, *1–6*, pp. 064306, 2009.
33. M. BULJAN, J. GRENZER, V. HOLÝ, N. RADIĆ, T. MIŠIĆ-RADIĆ, S. LEVICHEV, S. BERNSTORFF, B. PIVAC, I. CAPAN, *Structural and charge trapping properties of two bilayer $(Ge+SiO_2)/SiO_2$ films deposited on rippled substrate*, Appl. Phys. Lett., **97**, *1–3*, pp. 163117, 2010.
34. M. DRAGHICI, M. MIU, V. IANCU, A. NASSIOPOULOU, I. KLEPS, A. ANGELESCU, M.L. CIUREA, *Oxidation-induced modifications of traps parameters in nanocrystalline porous silicon*, Phys. Stat. Sol. (a), **182**, pp. 239–243, 2000.
35. M.L. CIUREA, M. DRAGHICI, V. IANCU, M. RESHOTKO, I. BALBERG, *Coupled confinement effect on the photoluminescence and electrical transport in porous silicon*, J. Luminesc., **102-103**, pp. 492–497, 2003.
36. M.L. CIUREA, *Electrical properties of nanocrystalline silicon*, J. Optoelectron. Adv. Mater., **8**, pp. 13–19, 2006.
37. V. IOANNOU-SOUGLERIDIS, V. TSAKIRI, A. G. NASSIOPOULOU, F. BASSANI, S. MENARD, F. ARNAUD D'AVITAYA, *Dielectric properties of nc-Si/CaF_2 multi quantum wells*, Mater. Sci. Eng. B, **69-70**, pp. 309–313, 2000.
38. V. IOANNOU-SOUGLERIDIS, A.G. NASSIOPOULOU, M.L. CIUREA, F. BASSANI, F. ARNAUD D' AVITAYA, *Trapping levels in nc-Si/CaF_2 multi-quantum-wells*, Mater. Sci. Eng. C, **15**, pp. 45–47, 2001.
39. M.L. CIUREA, V. IANCU, S. LAZANU, A.-M. LEPADATU, E. RUSNAC, I. STAVARACHE, *Defects in silicon: from single crystals to nanostructures*, Rom. Rep. Phys., **60**, pp. 735–748, 2008.
40. M.L. CIUREA, M. DRAGHICI, S. LAZANU, V. IANCU, A. NASIOPOULOU, V. IOANNOU, V. TSAKIRI, *Trapping levels in nanocrystalline porous silicon*, Appl. Phys. Lett., **76**, pp. 3067–3069, 2000.
41. V. IANCU, M.L. CIUREA, M. DRAGHICI, *Modeling of optical charging spectroscopy investigation of trapping phenomena in nanocrystalline porous silicon*, J. Appl. Phys., **94**, pp. 216–223, 2003.
42. A.-M. LEPADATU, I. STAVARACHE, S. LAZANU, V. IANCU, M.R. MITROI, R.R. NIGMATULIN, M.L. CIUREA, *Temperature dependence of capture coefficients in trapping phenomena*, CAS: 2010 International Semiconductor Conference Proceedings, Book Series International Semiconductor Conference, IEEE, **1**, pp. 371–374, 2010.

Received August 25, 2011